THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 19

UNITED STATES PATENT AND TRADEMARK OFFICE

_____

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

_____

Ex parte JAVIER F. IZQUIERDO and
JOHN A. LANDRY

_____

Appeal No. 96-1152
Application 08/001,091[1]

_____

ON BRIEF

_____

Before THOMAS, JERRY SMITH and CARMICHAEL, Administrative Patent Judges.

THOMAS, Administrative Patent Judge.

[1] Application for patent filed January 6, 1993. According to the appellants, this application is a continuation of Application 07/431,659, filed November 3, 1989, now U.S. Patent 5,201,055, issued April 6, 1993.

DECISION ON APPEAL

Appellants have appealed to the Board from the examiner's final rejection of claims 1 to 10, which constitute all the claims in the application.

Representative claim 1 is reproduced below:

1. A method operable by an electronic device for selecting one of a plurality of devices each having a data width and which are addressed using a first number of address lines, wherein each of the devices is coupled to a data bus having a data width, and wherein the data width of each device is less than or equal to the data bus width, the method comprising:

decoding said first number of address lines to produce a plurality of signals each representing selection of a different one of the devices;

encoding said plurality of selection representing signals into a set of addressing signals having an encoded value wherein each encoded value represents a different one of the devices and the number of signals in said set is less than said first number;

decoding said encoded set of addressing signals to produce a signal representing selection of one of the devices; and

selecting the device using said selection signal.

The following reference is relied on by the examiner:

| | | |
|---|---|---|
| Baker et al. (Baker) | 5,119,292 | June 2, 1992 (filed July 21, 1989) |

Claims 1 to 10 stand rejected under 35 U.S.C. § 103.[2] As evidence of obviousness, the examiner relies upon Baker alone.

Rather than repeat the positions of the appellants and the examiner, reference is made to the various briefs and answers for the respective details thereof.

OPINION

At the outset, we note that page 3 of the answer indicates the examiner relies upon the final rejection and an earlier Office action for the statement of the rejection of the present claims on appeal. Page 2 of the final rejection itself incorporates by reference this prior Office action. This approach of the examiner violates MPEP § 1208, Topic A, which permits the examiner to rely upon a single Office action for a statement of the rejection and instructs the examiner to avoid multiple references to other Office actions.

Essentially, for the reasons set forth by the appellants in the various briefs, we reverse the outstanding rejection of all claims on appeal under 35 U.S.C. § 103. There are various reasons for this conclusion.

[2] An additional prior art rejection under 35 U.S.C. § 103 based on a reference to Thomas has been withdrawn at page 3 of the answer.

We do not agree with the examiner's view that the preamble of each independent claim on appeal shows only an area of interest and that the body must therefore recite the limitations in the preamble. As expressed at pages 21 and 22 of the principal Brief on appeal, the body of each independent claim refers back to language specifically recited in the preamble of each independent claim to aid in defining certain device and bus features. As such, the recitations in the preamble cannot be ignored.

The examiner's view that the T1 signal is used as a processor active signal (broadly interpreted) as expressed at the bottom of page 5 of the Office action mailed on July 30, 1993 is misplaced. The examiner has provided no evidence beyond conjecture that this feature of independent claim 10, the only independent claim that relates to a processor activation signal, is present in Baker in any manner. Furthermore, we are aware of no such teaching. Therefore, there would appear to be no basis in Baker to meet the feature of independent claim 10 on appeal of "utilizing said processor active signal to decode said encoded set of signals to produce a second signal representing selection of a device."

The examiner asserts that the initial decoding operation in each independent claim on appeal is met by the address decoding logic 796 in Fig. 24. The discussion of this circuit at the bottom of col. 75, between lines 52 and 58 indicates that address decoding logic 796 "produces corresponding output values on a plurality of device-addressed lines. These device-addressed lines indicate whether the values currently on the data lines correspond to an address associated with the COM device's various address spaces." These various address spaces are discussed in detail for each of the named lines at col. 76 which, as asserted by appellants generally indicate that the total effective data widths of the devices that are referenced in this decoder are larger than the data widths of the system data bus of the claims on appeal. Thus, we are in a general agreement with the appellants general observation at the bottom of page 20 of the principal Brief on appeal that other address lines must be used to aid in the address decoding process.

After our study of Baker as well as the positions presented by both appellants and the examiner, we are in general agreement with the statement at the top of page 3 of the reply brief, filed on April 4, 1995:

> As claimed, the device having a data width less than the data width of the bus is

> not the device selection signal itself, as apparently asserted by the Examiner, but the device that is selected by the selection signal. In Baker, the 8 device selection signals (which Applicants have assumed are decoded from the 3-bit signal BCI_SCN[2:0]) are used to select one of a plurality of devices each having a data width that is much larger than the data width of the bus BI_D[31:0]. This is contrary to the requirements specified in claims 1 and 6 that "the data width of each device is less than or equal to the data bus width." Therefore, Baker does not teach or suggest selection of a device that has a data width less than or equal to the data bus width.

BCI_SCN signals outputted from the circuit in Fig. 24 in Baker do appear to be 3 binary bit positions as expressed at the top four lines of col. 78 of Baker as they relate to the showing in Fig. 25.

Because we find that the recitations of the various features in each independent claim 1, 6 and 10 on appeal are much more specific than those asserted from the teachings and showings the examiner has found to correspond in Baker and because we find that the claims would not have been otherwise obvious over those teachings and showings identified by the examiner in Baker, we reverse the rejection of claims 1 to 10 under 35 U.S.C. § 103.

REVERSED

| | |
|---|---|
| JAMES D. THOMAS<br>Administrative Patent Judge | ) |
| JERRY SMITH<br>Administrative Patent Judge | ) BOARD OF PATENT<br>)<br>) APPEALS AND<br>)<br>) INTERFERENCES |
| JAMES T. CARMICHAEL<br>Administrative Patent Judge | ) |

sd

Keith Lutsch
Pravel, Hewitt, Kimball and Krieger
1177 West Loop South
10th Floor
Houston, TX 77027-9095